layer of dielectric 26 is then deposited, on the last layer of metal 24, and holes opened 27 to the contact points of metal layer.

A layer of solder is deposited by electroplating, screen printing or ball mounting and contacts are made through the etched holes in the insulating layer to the final metal layer. The solder is then reflowed to form the solder bumps 28. Alternately, gold bumps may be used, as is known in the art.

In the Claims:

Please Amend Claim 39 as follows:

39. (AMENDED) A method for fabricating a thin film semiconductor die package, comprising the steps of:

providing a planar glass substrate;

attaching semiconductor dies to said planar glass substrate;

forming a polymer layer overlying said planar glass substrate and filling gaps between said semiconductor die;

thereafter depositing a dielectric layer overlying said polymer layer and said semiconductor die;

patterning said dielectric layer to form openings to said semiconductor die;

forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

forming a layer of solder over and connected to said metal interconnect layer; and

reflowing the solder to form solder bumps.

Please Cancel Claim 40.

Please Amend Claim 41 as follows:

41. (AMENDED) A method of fabricating a thin film semiconductor die package structure comprising:

providing a metal substrate;

forming a patterned glass layer overlying said metal substrate wherein said patterned glass layer has openings exposing said metal substrate;

attaching semiconductor die to said exposed metal substrate;

depositing a dielectric layer overlying said patterned

glass layer and said semiconductor die;

patterning said dielectric layer to form openings to said semiconductor die;

forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

forming a layer of solder over and connected to said metal interconnect layer; and

reflowing the solder to form solder bumps.

Please Amend Claim 42 as follows:

42. (AMENDED) A method of fabricating a thin film semiconductor die package structure comprising:

providing a first glass substrate with semiconductor dies mounted on said first glass substrate wherein the active surface of said semiconductor dies is facing said first glass substrate;

filling polymer or epoxy between and over the backside of said semiconductor dies;

grinding the planarized surface and said backside of said semiconductor dies;

mounting a second glass substrate on the backside of the semiconductor dies;

grinding the first glass substrate;

etching holes in said first glass substrate to expose said semiconductor dies;

sequentially forming polymer insulating layers and metal interconnect layers over said first glass substrate;

depositing a layer of solder over and connected to a topmost said metal interconnect layer; and

reflowing the solder to from solder bumps.

Please Cancel Claims 43 and 44.

Please Amend Claim 49 as follows:

49. (AMENDED) The method of claim 42 wherein the solder bumps are connected to said interconnect metal and are further incorporated as interconnects to the next level of assembly.

Please Cancel Claim 50.

Please Amend Claim 53 as follows:

53. (AMENDED) A method of fabricating a thin film semiconductor die package structure comprising:

providing a first glass substrate with semicondutor dies mounted on said first glass substrate wherein the active surface of said semiconductor dies is facing said first glass substrate;

filling polymer or epoxy between and over the backside of said semiconductor dies;

grinding the planarized surface, and said backside of said semiconductor dies;

mounting a second glass substrate on the backside of the semiconductor dies;

removing said first glass substrate;

sequentially forming polymer insulating layers and metal interconnect layers over said semiconductor dies;

depositing a layer of solder over and connected to a topmost said metal interconnect layer; and

reflowing the solder to form solder bumps.

REMARKS

Examiner A. Chambliss is thanked for the thorough examination and search of the subject Patent Application. Claims

39, 41, 42, 49, and 53 have been amended. Claims 40, 43, 44, and 50 have been canceled. The Specification title, page 4, and page 7 has been amended. Drawing Fig. 1e has been amended and is attached (attachment A).

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the objection to the drawings because Figs. 4k, 4l, and 5l are not in the brief description of the drawings is requested based on the amendment of the Specification, page 4, and on the following remarks.

Page 4 has been amended to reference the cited drawings.

Reconsideration of the objection to the drawings because Figs. 4k, 4l, and 5l are not in the brief description of the drawings is requested based on the amendment of the Specification, page 4, and on the above remarks.

Reconsideration of the objection to the drawings because they do not include reference signs mentioned in the description and because they include references not mention in the

description is requested based on the amendment of the Specification, page 7, on the amended to the drawings, and on the following remarks.

Drawing Fig. 1e has been amended to include the reference sign 20 for the second dielectric layer as described in the original application on page 6, line 17. In addition, the reference sign 27 (in Fig. 1g) clearly refers to a contact opening as is referred to in the phrase "holes opened to the contact points of metal layer" found in the original specification. The reference number "27" was inadvertently left off. The phrase has been amended to read: "holes opened ***27*** to the contact points of metal layer." The above amendments should overcome the objection.

Reconsideration of the objection to the drawings because they do not include reference signs mentioned in the description and because they include references not mention in the description is requested based on the amendment of the Specification, page 7, on the amendment to the drawings, and on the above remarks.

Reconsideration of the objection to the drawings because they do not show every feature of the invention specified in the claims is requested based on Canceled Claim 50 and on the following remarks.

Claim 50 referenced the connector pins and has been canceled.

Reconsideration of the objection to the drawings because they do not show every feature of the invention specified in the claims is requested based on Canceled Claim 50 and on the above remarks.

Reconsideration of the objection to the Specification because the title is not descriptive is requested based on the Amended Title and on the following remarks.

The title has been amended as requested.

Reconsideration of Claims 40-58 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested based

Amended Claims 41, 42, 49, and 53, Canceled Claims 40, 43, 44, and 50, and on the following remarks.

In regards to (9) in Claim 40, 41, the vague phrase "forming polymer layers and metal interconnect layers" has been removed from Claim 41 and replaced with more definitive terminology as shown by:

[sequentially forming polymer insulating layers and metal interconnect layers;]

depositing a dielectric layer overlying said patterned glass layer and said semiconductor die;

patterning said dielectric layer to form openings to said semiconductor die;

forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

Claim 40 has been canceled. The above changes should resolve the problem described by (9).

In regards to (10) in Claims 40, 41, 42, and 53, the vague phrase "forming a solder layer" has been amended in Claims 41, 42, and 53 to read as follows (ex. Claim 41):

forming a layer of solder over and connected to said metal interconnect layer; and

Claim 40 has been canceled. The above changes should resolve the problem described by (10).

In regards to (11) in Claim 49 the limitation "solder bumps" has been amended to "the solder bumps" to provide antecedent basis.

In regards to (12) through (17) Applicant believes that the Examiner is referring to Claim 42 rather than Claim 41 and will focus comments on Claim 41 accordingly.

Specifically in regards to (12) in Claims 42 and 53 the vague phrase "to obtain a planarized surface" been removed.

In regards to (13) in Claim 42 the vague phrase "the desired thickness" has been removed from Amended Claim 42.

In regards to (14) in Claim 42 Applicant respectfully disagrees that the phrase "grinding the first glass substrate" is vague. Applicant has amended Claim 42 to make clear the references to

the first and second glass substrates. Further, Applicant draws the Examiner's attention to Figs. 4c - 4e. In Fig. 4c, the process step is shown where only the first glass substrate 38 is present. Note that the active sides of the die 12 are facing the substrate 38. Next, in Fig. 4d, a second glass substrate 10 is attached to the back sides of the die 12. Then in Fig. 4e, note that the drawing is inverted so that the first glass layer 38 is on top and the second glass layer 10 is on bottom. The first glass layer is then ground to reduce its thickness. These teachings are consistent with those of Amended Claim 42. Note that Amended Claim 42 further specifies that the active side of the die face the first glass substrate.

In regards to (15) in Claim 42 the vague phrase "a desired glass thickness" has been removed from Amended Claim 42.

In regards to (16) in Claim 42 Applicant respectfully disagrees that the phrase "etching holes in first glass substrate" is vague. As noted above in re (14), the drawing is inverted in Fig. 4e and remains so in Fig. 4f wherein the contact holes are formed.

In regards to (17) in Claim 42 Applicant respectfully disagrees that the phrase "forming polymer insulating layers and metal interconnect layers over said first glass substrate" is vague for the same reason cited in re (16).

Reconsideration of Claims 40-58 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested based Amended Claims 41, 42, 49, and 53, Canceled Claims 40, 43, 44, and 50, and on the following remarks.

Reconsideration of Claim 39 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Eichelberger (U.S. Patent 5,250,843) is requested based Amended Claim 39 and on the following remarks.

Applicant agrees that Eichelberger teaches a method to form integrated circuit packages. However, Eichelberger differs from the Claimed invention of Amended Claim 39 in two significant ways. First, Eichelberger teaches forming a polymer encapsulant 18 filling gaps between die 14 and then forms via holes 22

through this polymer layer 18. In contrast, Applicant teaches in Amended Claim 39:

> forming a polymer layer overlying said planar glass substrate and filling gaps between said semiconductor die;
>
> thereafter depositing a dielectric layer overlying said polymer layer and said semiconductor die;
>
> patterning said dielectric layer to form openings to said semiconductor die;
>
> forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

Therefore, it can be seen that Applicant's claimed invention, as recited in Amended Claim 39, differs substantially from the teachings of Eichelberger. In particular, Applicant first forms a polymer layer to fill between the die, then deposits a dielectric layer over the polymer layer and the die, then patterns the dielectric layer to form openings to the die for the formation of metal contacts. Because, Applicant's method as taught in Amended Claim 39 is substantially different than the teachings of Eichelberger, Eichelberger does not anticipate Applicant's invention.

Second, Applicant's invention as recited in Amended Claim 39 differs from Eichelberger with respect to the use of solder bumps. Applicant teaches the formation of solder bumps for interconnection as shown by:

> forming a layer of solder over and connected to said [one or more] metal interconnect <u>layer</u> [layers]; and
>
> reflowing the solder to form solder bumps.

However, Eichelberger teaches the use of button contacts 176 (Fig. 14) as noted by the Examiner. Button contacts are substantially different technology than solder bumps. An except from a product catalog from the Cinch Corporation has been taken from a Cinch corporate website addressable by: (www.cinch.com/products/cinapse/printable/index.html) This excerpt is attached to this amendment (attachment B). In the attachment, at page 2, paragraph 3, it states:

"The key to this high performance technology is the CIN::APSE® button-contact. The contacts are made by randomly winding gold plated molybdenum or tungsten wire into a cylindrical button. The buttons are then loaded (stitched) into a custom molded

insulator configured to the exact requirements of the application..."

The above-described button-contact technology is well-known to the art and represents a mechanical means of providing contact points on the die. This is a time consuming process that provides a minimum button contact size of only 0.5 mm which does not meat the requirements of high density packaging which is an objective of the present invention. In this respect, the teachings of Eichelberger are substantially different from those of Applicant's invention as recited in Amended Claim 39.

Reconsideration of Claim 39 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Eichelberger (U.S. Patent 5,250,843) is requested based Amended Claim 39 and on the above remarks.

Reconsideration of Claims 40 and 41 rejected under 35 U.S.C. 103(a) as unpatentable over Eichelberger (U.S. Patent 5,250,843) as applied to Claim 39 above and further in view of Neugebaurer et al (U.S. Patent 5,291,066) is requested based Amended Claim 41, Canceled Claim 40, and on the following remarks.

Applicant agrees that Neugebaurer teaches a method to form packaged integrated circuits. Neugebaurer shows a substrate 10 having cavities 11 cut for the placement of die 12. However, Applicant's invention, as recited in Amended Claim 41 teaches:

> providing a metal substrate;
>
> forming a patterned glass layer overlying said metal substrate wherein said patterned glass layer has openings exposing said metal substrate; [with cavities for mounting semiconductor dies on said metal substrate;]
>
> attaching semiconductor die to said exposed metal substrate;

Referring now to Figs. 3a-3d, note that a patterned glass layer is formed over a metal substrate 10 to form the composite substrate layer 36. It is the overlying glass layer that is patterned to form openings 34 for attaching the die 12 to the metal substrate 10. The metal substrate 10 is not patterned. Neugebaurer and Eichelberger do not teach or suggest, separately or in combination, the formation of the integrated circuit package in this way. Therefore, Amended Claim 41 should be patentable over Eichelberger (U.S. Patent 5,250,843) in view of

Neugebaurer et al (U.S. Patent 5,291,066). Claim 40 has been canceled.

Reconsideration of Claims 40 and 41 rejected under 35 U.S.C. 103(a) as unpatentable over Eichelberger (U.S. Patent 5,250,843) as applied to Claim 39 above and further in view of Neugebaurer et al (U.S. Patent 5,291,066) is requested based Amended Claim 41, Canceled Claim 40, and on the above remarks.

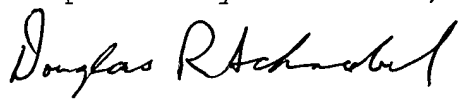
Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner A. Chambliss not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,



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